What Is Claimed Is:

1. A method for forming a semiconductor device isolating barrier comprising:

forming a pad oxide layer and a first nitride layer on a semiconductor substrate;

forming a trench region by etching the pad oxide layer and the first nitride layer;

forming spacers at sidewalls of the etched first nitride layer;

forming a first trench by etching the semiconductor substrate using the spacers and the etched first nitride layer as a mask; and

after forming a liner oxide layer and an oxide layer filling the first trench, forming the device isolating barrier by flattening the liner oxide layer and the trench oxide layer to expose the etched first nitride layer.

2. A method as defined in claim 1, wherein a thickness of the first nitride layer ranges from about 500 to about 1000 Å.

3. A method for forming a gate electrode of a semiconductor device comprising:

forming a pad oxide layer and a first nitride layer on a semiconductor substrate;

forming a trench region by etching the pad oxide layer and the first nitride layer;

forming spacers at sidewalls of the etched pad oxide layer;

forming a first trench by etching the semiconductor substrate using the spacers and the etched first nitride layer as a mask;

after forming a liner oxide layer and an oxide layer filling the trench, forming a device isolating barrier by flattening the liner oxide layer and the trench oxide layer to expose the etched first nitride layer;

after forming a second nitride layer on top of the etched first nitride layer, forming a second trench by etching the second nitride layer and the etched first nitride layer;

after a conducting layer is formed to fill the second trench, flattening the conducting layer to expose the second nitride layer; and

forming the gate electrode by removing the second nitride layer and the etched first nitride layer.

4. A method as defined in claim 3, wherein a thickness of the first nitride layer ranges from about 500 to about 1000 Å.

5. A method as defined in claim 3, wherein a thickness of the second nitride layer ranges from about 1000 to about 1500 Å.

6. A method as defined in claim 3, wherein an etching gas used in removing the second nitride layer and the etched first nitride layer has a greater than a 7 : 1 selectivity of the first and the second nitride layer with respect to the oxide layer.

7. A method as defined in claim 6, wherein the etching gas is a mixture of CO, CHF_3 and C_4F_8.

8. A method as defined in claim 3, wherein the conducting layer deposited to fill the second trench is formed through a LPCVD process at about 550 to about 650 ℃.

9. A method as defined in claim 8, wherein a thickness of the deposited conducting layer ranges from 2000 to 5000 Å.

10. A method as defined in claim 3, wherein flattening the conducting layer comprises performing a chemical mechanical polishing process, and wherein a thickness of the nitride layer left after the flattening process ranges from about 10 to about 90 % of a thickness of the nitride layer before the flattening.